查询ST93CS66供应商

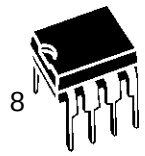
SGS-THOMSON MICROELECTRONICS

ST93CS66
ST93CS67

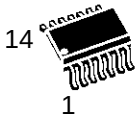
4K (256 x 16) SERIAL MICROWIRE EEPROM

NOT FOR NEW DESIGN

- 1 MILLION ERASE/WRITE CYCLES, with 40 YEARS DATA RETENTION
- SELF-TIMED PROGRAMMING CYCLE with AUTO-ERASE
- READY/BUSY SIGNAL DURING PROGRAMMING
- SINGLE SUPPLY VOLTAGE
  - 3V to 5.5V for the ST93CS66
  - 2.5V to 5.5V for the ST93CS67
- USER DEFINED WRITE PROTECTED AREA
- PAGE WRITE MODE (4 WORDS)
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME
- ***ST93CS66 and ST93CS67 are replaced by the M93S66***



PSDIP8 (B)
0.25mm Frame



SO14 (ML)
150mil Width

DESCRIPTION

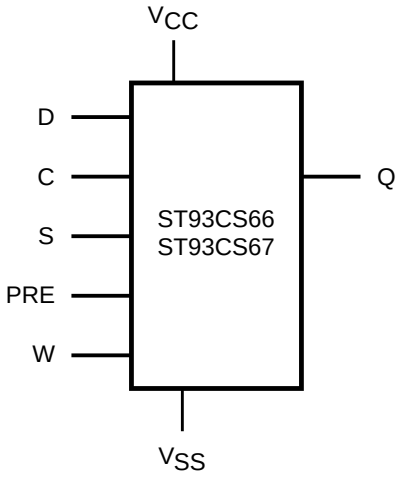
The ST93CS66 and ST93CS67 are 4K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed through a serial input D and output Q.

The 4K bit memory is organized as 256 x 16 bit words.The memory is accessed by a set of instructions which include Read, Write, Page Write, Write All and instructions used to set the memory protection. A Read instruction loads the address of the first word to be read into an internal address pointer.

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
PRE	Protect Enable
W	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



This is information on a product still in production but not recommended for new designs.

Figure 2A. DIP Pin Connections

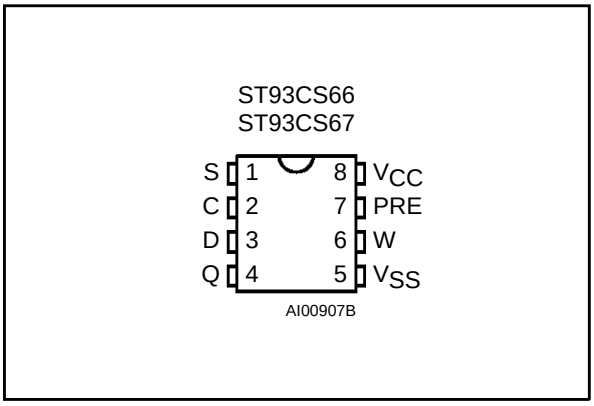
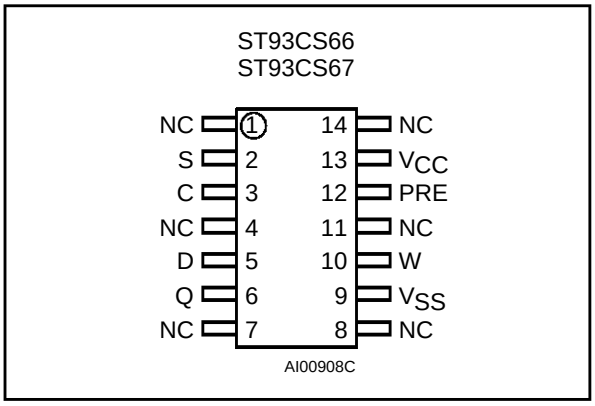


Figure 2B. SO Pin Connections



Warning: NC = Not Connected.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature			–40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO14 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages (Q = V_{OH} or Hi-Z)			–0.3 to V_{CC} +0.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			2000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

The data is then clocked out serially. The address pointer is automatically incremented after the data is output and, if the Chip Select input (S) is held High, the ST93CS66/67 can output a sequential stream of data words. In this way, the memory can be read as a data stream of 16 to 4096 bits, or continuously as the address counter automatically rolls over to 00 when the highest address is reached.

Within the time required by a programming cycle (t_W), up to 4 words may be written with the help of the Page Write instruction; the whole memory may also be erased, or set to a predetermined pattern, by using the Write All instruction.

Within the memory, an user defined area may be protected against further Write instructions. The size of this area is defined by the content of a Protect Register, located outside of the memory array. As a final protection step, data may be permanently protected by programming a One Time Programing bit (OTP bit) which locks the Protect Register content.

Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction. The Write instruction writes 16 bits at one time into one of the 256 words, the Page Write instruction writes up to 4 words of 16 bits to sequential locations, assuming in both cases that all addresses are outside the Write Protected area. After the start of the programming cycle, a Ready/Busy signal is available on the Data output (Q) when the Chip Select (S) input pin is driven High.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

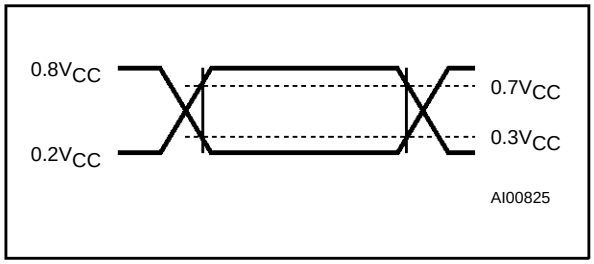


Table 3. Capacitance (1)
(T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: 1. Sampled only, not 100% tested.

Table 4. DC Characteristics (T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3V to 5.5V for ST93CS66 and V_{CC} = 2.5V to 5.5V for ST93CS67)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = V_{SS}, C = V_{SS}		50	µA
V_{IL}	Input Low Voltage (ST93CS66,67)	$4.5V \le V_{CC} \le 5.5V$	–0.1	0.8	V
	Input Low Voltage (ST93CS66)	$3V \le V_{CC} \le 5.5V$	–0.1	0.2 V_{CC}	V
	Input Low Voltage (ST93CS67)	$2.5V \le V_{CC} \le 5.5V$	–0.1	0.2 V_{CC}	V
V_{IH}	Input High Voltage (ST93CS66,67)	$4.5V \le V_{CC} \le 5.5V$	2	V_{CC} + 1	V
	Input High Voltage (ST93CS66)	$3V \le V_{CC} \le 5.5V$	0.8 V_{CC}	V_{CC} + 1	V
	Input High Voltage (ST93CS67)	$2.5V \le V_{CC} \le 5.5V$	0.8 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 5. AC Characteristics (T_A = 0 to 70° or, –40 to 85°C; V_{CC} = 3V to 5.5V for ST93CS66 and V_{CC} = 2.5V to 5.5V for ST93CS67)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High		50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High		50		ns
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition		100		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low			500	ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid			500	ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition		0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition		250		ns
t_{CLSL}	t_{CSH}	Clock Low to Chip Select Transition		0		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid			500	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z			300	ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.
2. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns.

Figure 4. Synchronous Timing, Start and Op-Code Input

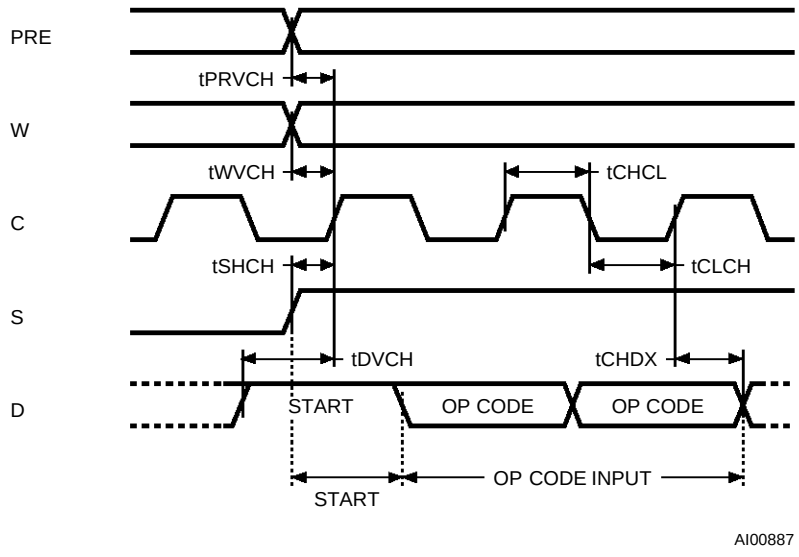
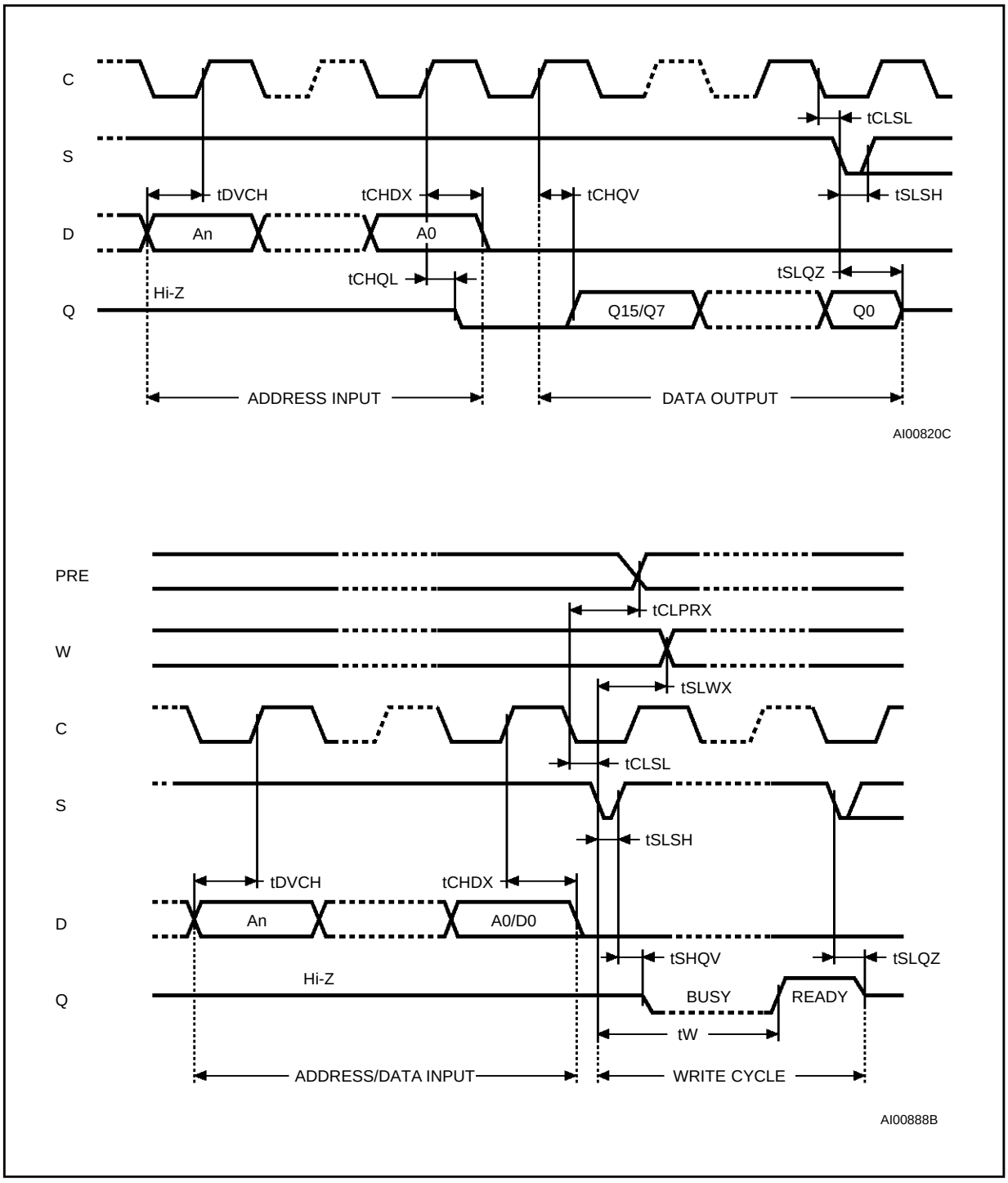


Figure 5. Synchronous Timing, Read or Write



POWER-ON DATA PROTECTION

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit resets all internal programming circuitry and sets the device in the Write Disable mode. When V_{CC} reaches its functional value, the device is properly reset (in the Write Disable mode) and is ready to decode and execute an incoming instruction. A stable V_{CC} must be applied before any logic signal.

INSTRUCTIONS

The ST93CS66/67 has eleven instructions, as shown in Table 6. Each instruction is composed of a 2 bit op-code and an 8 bit address. Each instruction is preceded by the rising edge of the signal applied on the Chip Select (S) input (assuming that the Clock C is low). The data input D is then sampled upon the following rising edges of the clock C until a '1' is sampled and decoded by the ST93CS66/67 as a Start bit.

The ST93CS66/67 is fabricated in CMOS technology and is therefore able to run from zero Hz (static input signals) up to the maximum ratings (specified in Table 5).

Read

The Read instruction (READ) outputs serial data on the Data Output (Q). When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 16 bit word with the MSB first.

Table 6. Instruction Set

Instruction	Description	W pin (1)	PRE pin	Op Code	Address (1)	Data	Additional Information
READ	Read Data from Memory	X	'0'	10	A7-A0	Q15-Q0	
WRITE	Write Data to Memory	'1'	'0'	01	A7-A0	D15-D0	Write is executed if the address is not inside the Protected area
PAWRITE	Page Write to Memory	'1'	'0'	11	A7-A0	D15-D0	Write is executed if all the addresses are not inside the Protected area
WRALL	Write All Memory	'1'	'0'	00	01XX XXXX	D15-D0	Write all data if the Protect Register is cleared
WEN	Write Enable	'1'	'0'	00	11XX XXXX		
WDS	Write Disable	X	'0'	00	00XX XXXX		
PRREAD	Protect Register Read	X	'1'	10	XXXX XXXX	Q8-Q0	Data Output = Protect Register content + Protect Flag bit
PRWRITE	Protect Register Write	'1'	'1'	01	A7-A0		Data above specified address A7-A0 are protected
PRCLEAR	Protect Register Clear	'1'	'1'	11	1111 1111		Protect Flag is also cleared (cleared Flag = 1)
PREN	Protect Register Enable	'1'	'1'	00	11XX XXXX		
PRDS	Protect Register Disable	'1'	'1'	00	0000 0000		OTP bit is set permanently

Note: 1. X = don't care bit.

Output data changes are triggered by the Low to High transition of the Clock (C). The ST93CS66/67 will automatically increment the address and will clock out the next word as long as the Chip Select input (S) is held High. In this case the dummy '0' bit is NOT output between words and a continuous stream of data can be read.

Write Enable and Write Disable

The Write Enable instruction (WEN) authorizes the following Write instructions to be executed, the Write Disable instruction (WDS) disables the execution of the following Erase/Write instructions. When power is first applied, the ST93CS66/67 enters the Disable mode. When the Write Enable instruction (WEN) is executed, Write instructions remain enabled until a Write Disable instruction (WDS) is executed or if the Power-on reset circuit becomes active due to a reduced V_{CC}. To protect the memory contents from accidental corruption, it is advisable to issue the WDS instruction after every write cycle.

The READ instruction is not affected by the WEN or WDS instructions.

Write

The Write instruction (WRITE) is followed by the address and the word to be written. The Write Enable signal (W) must be held high during the WRITE instruction. Data input D is sampled on the Low to High transition of the clock. After the last data bit has been sampled, Chip Select (S) must be brought Low before the next rising edge of the clock (C), in order to start the self-timed programming cycle, providing that the address is NOT in the protected area. If the ST93CS66/67 is still performing the programming cycle, the Busy signal (Q = 0) will be returned if the Chip Select input (S) is driven high, and the ST93CS66/67 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93CS66/67 is ready to receive a new instruction.

Page Write

A Page Write instruction (PAWRITE) contains the first address to be written followed by up to 4 data words. The Write Enable signal (W) must be held High during the Write instruction. Input address and data are read on the Low to High transition of the clock. After the receipt of each data word, bits A1-A0 of the internal address register are incremented, the high order bits A7-A2 remaining unchanged. Users must take care by software to ensure that the last word address has the same six upper order address bits as the initial address transmitted to avoid address roll-over.

After the LSB of the last data word, Chip Select (S) must be brought Low before the next rising edge of the Clock (C). The falling edge of Chip Select (S) initiates the internal, self-timed write cycle. The Page Write operation will not be performed if any of the 4 words is addressing the protected area. If the ST93CS66/67 is still performing the programming cycle, the Busy signal (Q = 0) will be returned if the Chip Select input (S) is driven high, and the ST93CS66/67 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93CS66/67 is ready to receive a new instruction.

Write All

The Write All instruction (WRALL) is valid only after the Protect Register has been cleared by executing a PRCLEAR (Protect Register Clear) instruction. The Write All instruction simultaneously writes the whole memory with the same data word included in the instruction. The Write Enable signal (W) must be held High before and during the Write instruction. Input address and data are read on the Low to High transition of the clock. If the ST93CS66/67 is still performing the programming cycle, the Busy signal (Q = 0) will be returned if the Chip Select input (S) is driven high, and the ST93CS66/67 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93CS66/67 is ready to receive a new instruction.

MEMORY WRITE PROTECTION AND PROTECT REGISTER

The ST93CS66/67 offers a Protect Register containing the bottom address of the memory area which has to be protected against write instructions. In addition to this Protect Register, two flag bits are used to indicate the Protect Register status: the Protect Flag enabling/disabling the protection of the Protect Register and the OTP bit which, when set, disables access to the Protect Register and thus prevents any further modifications of this Protect Register value. The content of the Protect Register is defined when using the PRWRITE instruction, it may be read when using the PRREAD instruction. A specific instruction PREN (Protect Register Enable) allows the user to execute the protect instructions PRCLEAR, PRWRITE and PRDS; this PREN instruction being used together with the signals applied on the input pins PRE (Protect Register Enable pin) and W (Write Enable).

Figure 6. READ, WRITE, WEN, WDS Sequences

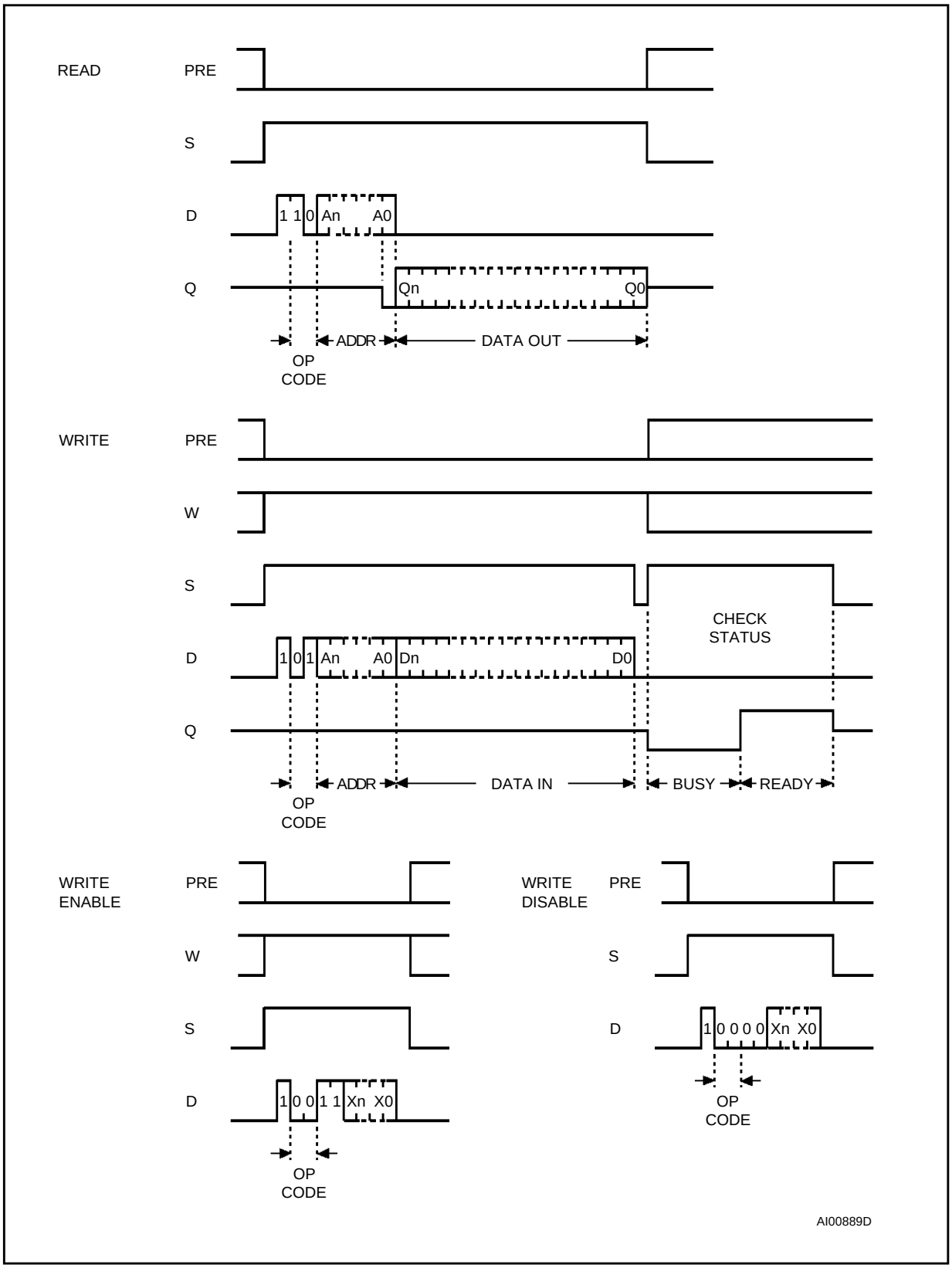
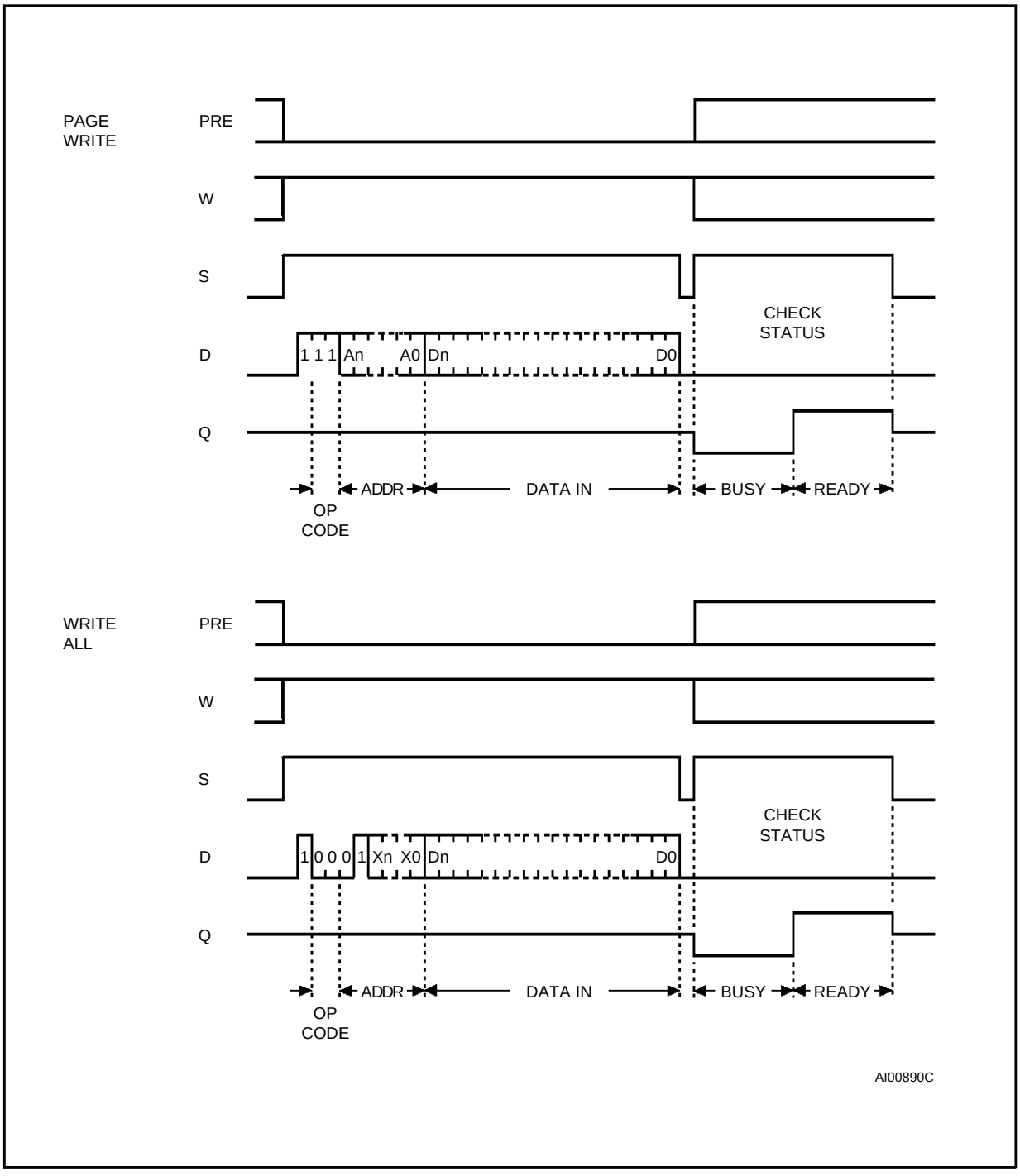


Figure 7. PAWRITE, WRALL Sequences



MEMORY WRITE PROTECTION (cont'd)

Accessing the Protect Register is done by executing the following sequence:

– WEN: execute the Write Enable instruction,
– PREN: execute the PREN instruction,
– PRWRITE, PRCLEAR or PRDS: the protection then may be defined, in terms of size of the protected area (PRWRITE, PRCLEAR) and may be set permanently (PRDS instruction).

Protect Register Read

The Protect Register Read instruction (PRREAD) outputs on the Data Output Q the content of the Protect Register, followed by the Protect Flag bit. The Protect Register Enable pin (PRE) must be driven High before and during the instruction. As in the Read instruction a dummy '0' bit is output first.

Since it is not possible to distinguish if the Protect Register is cleared (all 1's) or if it is written with all 1's, user must check the Protect Flag status (and not the Protect Register content) to ascertain the setting of the memory protection.

Protect Register Enable

The Protect Register Enable instruction (PREN) is used to authorize the use of further PRCLEAR, PRWRITE and PRDS instructions. The PREN insruction does not modify the Protect Flag bit value.

Note: A Write Enable (WEN) instruction must be executed before the Protect Enable instruction. Both the Protect Enable (PRE) and Write Enable (W) input pins must be held High during the instruction execution.

Protect Register Clear

The Protect Register Clear instruction (PRCLEAR) clears the address stored in the Protect Register to all 1's, and thus enables the execution of WRITE and WRALL instructions. The Protect Register Clear execution clears the Protect Flag to '1'. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution.

Note: A PREN instruction must immediately precede the PRCLEAR instruction.

Protect Register Write

The Protect Register Write instruction (PRWRITE) is used to write into the Protect Register the address of the first word to be protected. After the PRWRITE instruction execution, all memory locations equal to and above the specified address, are protected from writing. The Protect Flag bit is set to '0', it can be read with Protect Register Read instruction. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution.

Note: A PREN instruction must immediately precede the PRWRITE instruction, but it is not necessary to execute first a PRCLEAR.

Protect Register Disable

The Protect Register Disable instruction sets the One Time Programmable bit (OTP bit). The Protect Register Disable instruction (PRDS) is a ONE TIME ONLY instruction which latches the Protect Register content, this content is therefore unalterable in the future. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution. The OTP bit cannot be directly read, it can be checked by reading the content of the Protect Register (PRREAD instruction), then by writing this same value into the Protect Register (PRWRITE instruction): when the OTP bit is set, the Ready/Busy status cannot appear on the Data output (Q); when the OTP bit is not set, the Busy status appear on the Data output (Q).

A PREN instruction must immediately precede the PRDS instruction.

READY/BUSY Status

When the ST93CS66/67 is performing the write cycle, the Busy signal (Q = 0) is returned if S is driven high, and the ST93CS66/67 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate, if S is driven high, that the ST93CS66/67 is ready to receive a new instruction. Once the ST93CS66/67 is Ready, the Data Output Q is set to '1' until a new Start bit is decoded or the Chip Select is brought Low.

COMMON I/O OPERATION

The Data Output (Q) and Data Input (D) signals can be connected together, through a current limiting resistor, to form a common, one wire data bus. Some precautions must be taken when operating the memory with this connection, mostly to prevent a short circuit between the last entered address bit (A0) and the first data bit output by Q. The reader should refer to the SGS-THOMSON application note "MICROWIRE EEPROM Common I/O Operation".

Figure 8. PRREAD, PRWRITE, PREN Sequences

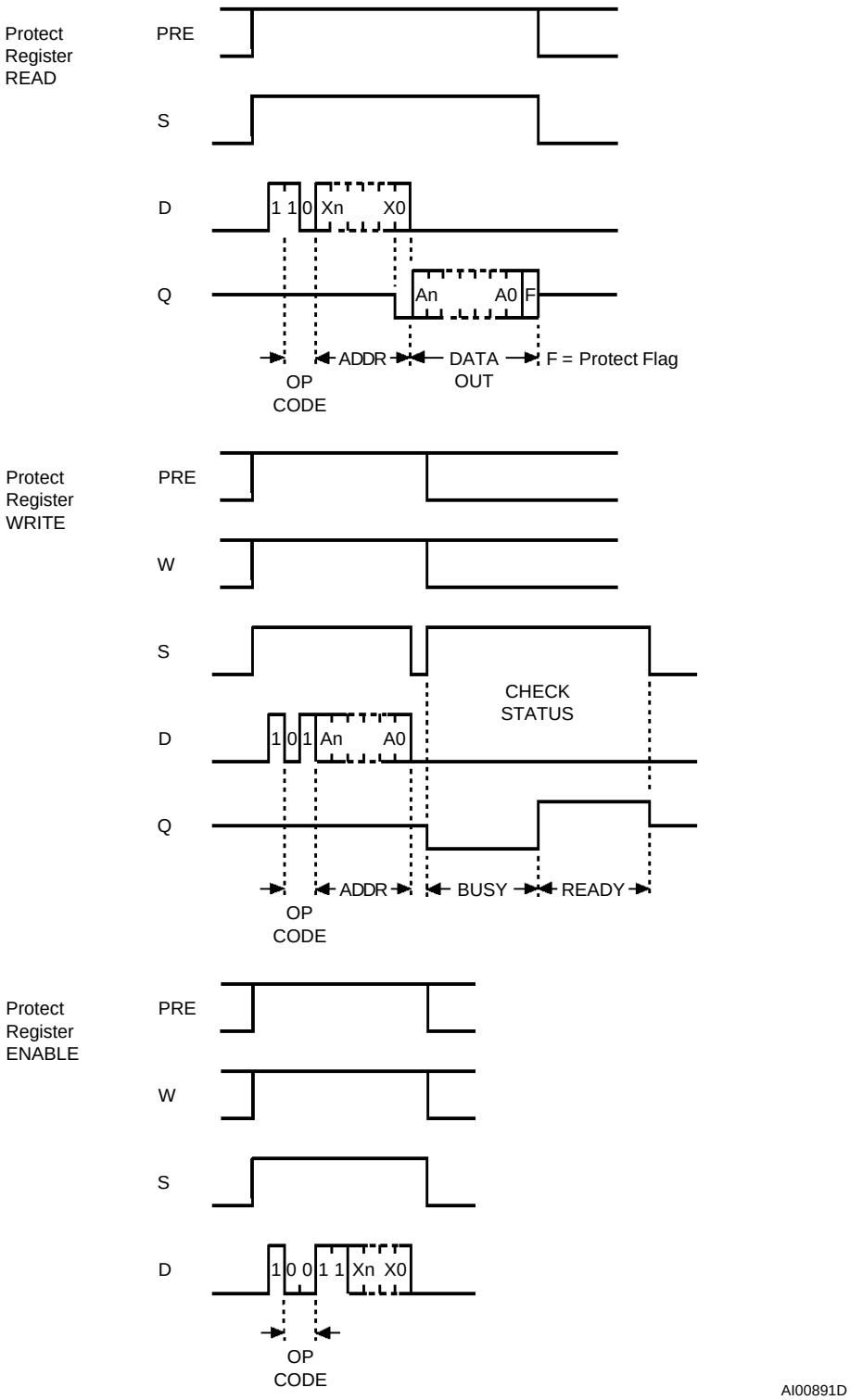
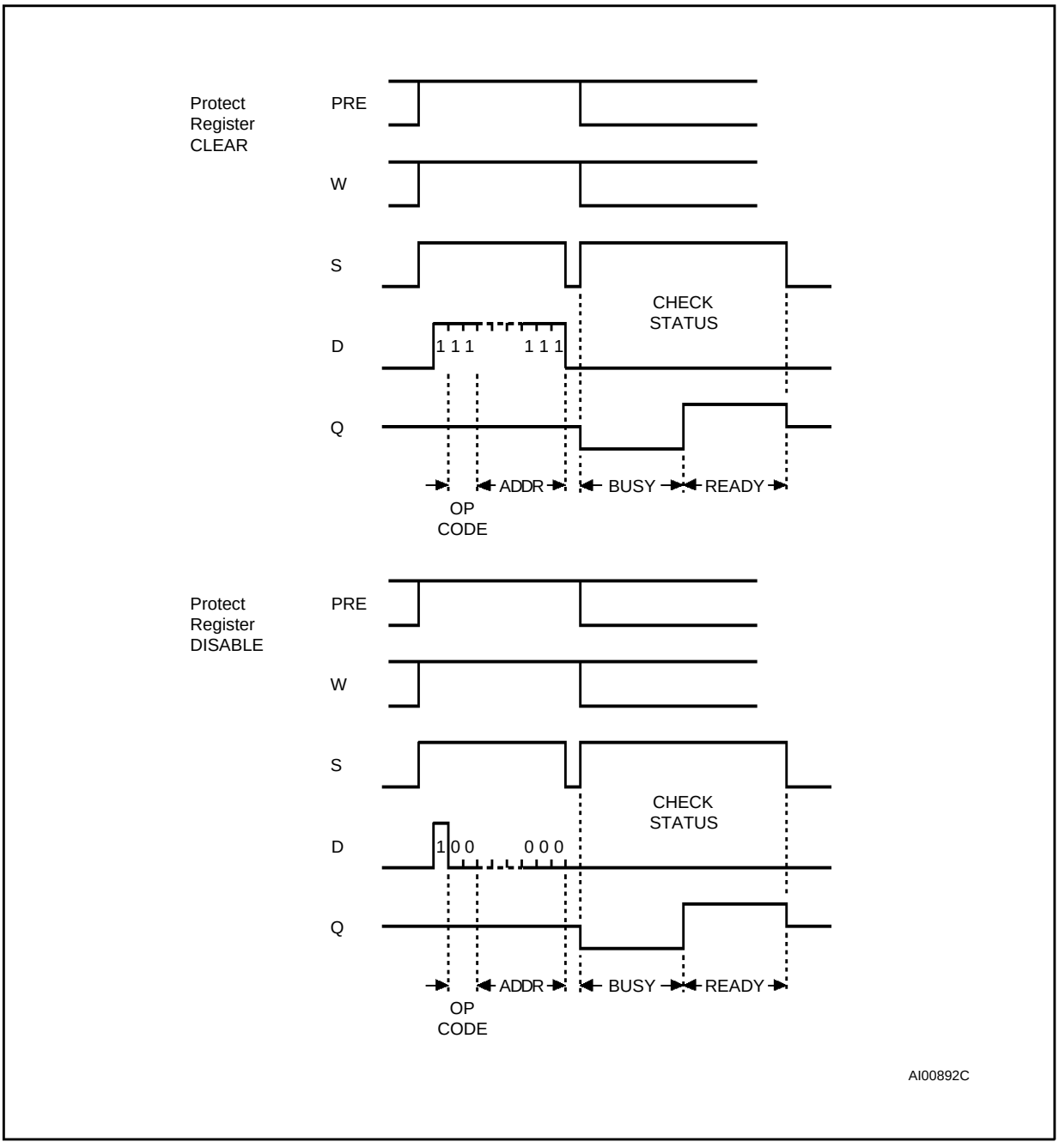
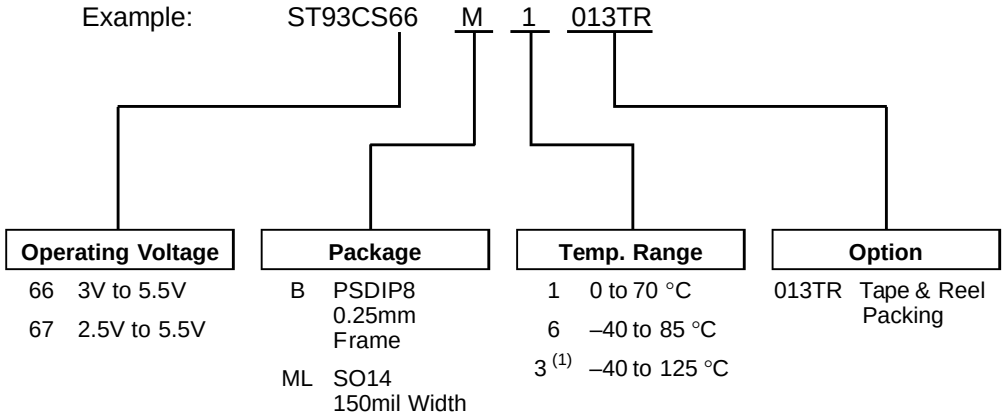


Figure 9. PRCLEAR, PRDS Sequences



ORDERING INFORMATION SCHEME



Note: 1. Temperature range on request only.

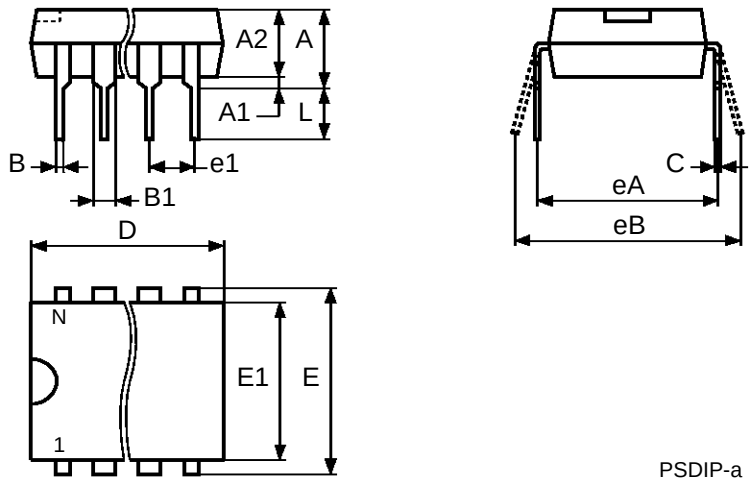
Devices are shipped from the factory with the memory content set at all ”1’s” (FFFFh).

For a list of available options (Operating Voltage, Package, etc...) or for further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		
CP			0.10			0.004

PSDIP8



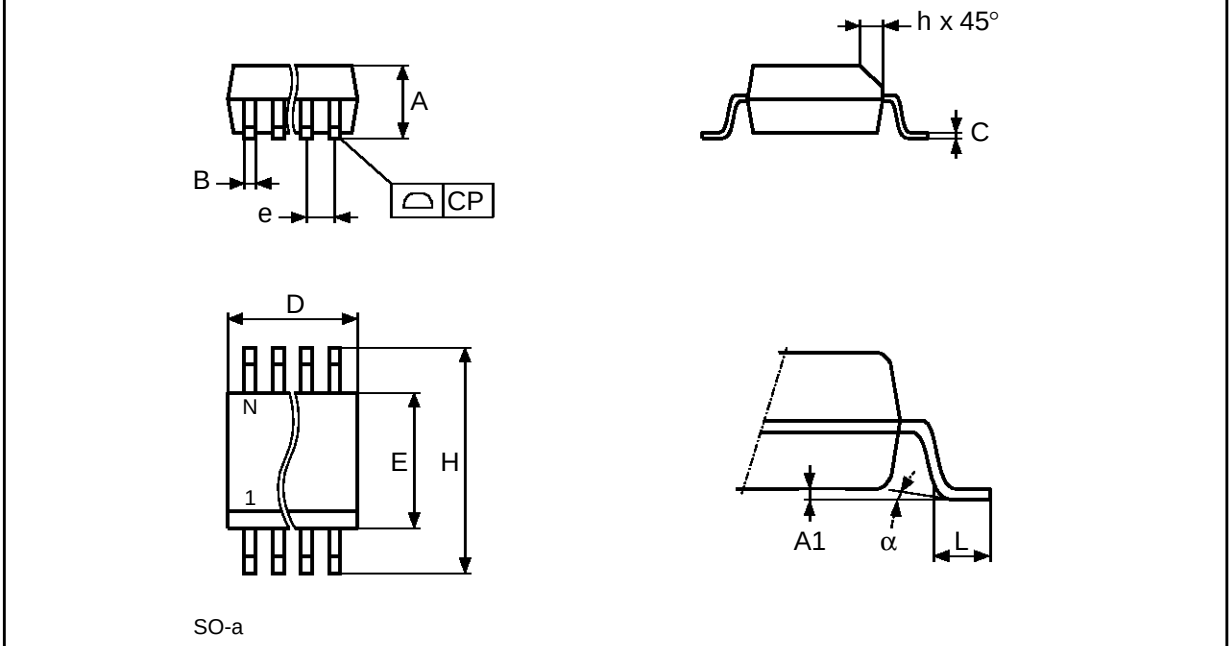
PSDIP-a

Drawing is not to scale

SO14 - 14 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		8.55	8.75		0.337	0.344
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.80		0.016	0.031
α		0°	8°		0°	8°
N	14			14		
CP			0.10			0.004

SO14



SO-a

Drawing is not to scale

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